A NEW PARADIGM FOR BASE STATION RECEIVERS: HIGH IF SAMPLING + DIGITAL FILTERING

by: Tom Gratzek, Brad Brannon, Jim Camp, and Frank Murden
Analog Devices - Communications Division
7910 Triad Center Drive
Greensboro, NC 27403
tom.gratzek @analog.com

Abstract
A dual-channel, IF sampling receiver IC with fast RSSI and AGC is described. The ADC samples with only 200 femto second aperture jitter and is used to digitize intermediate frequencies (IFs) up to 250 MHz. A companion digital filter and mixer processor provides 1657 MOPs; together they provide a flexible platform for use in a new generation of digital receivers for various radio standards.

1.0 Introduction

The worldwide cellular and PCS infrastructure build-out has provided market incentives to develop better radio receivers. Better means smaller, lower power dissipation, higher sensitivity, less factory tweaking, higher manufacturing yields, field programmability, and operational flexibility. Fortunately, advances in semiconductor technologies have continued so that new radio architectures can be developed that meet the goals of the "radio" industry. This paper discusses a new single channel diversity radio architecture that has recently been developed that can be applied to several open and proprietary radio standards.

In recent years, digital radios have replaced analog radios as a way to increase privacy, and use spectrum more efficiently. One dream has been to digitize at RF, then to sort everything out in a super digital radio CMOS chip. Recent semiconductor and chip architecture developments mave made real progress towards this vision possible. High IF sampling, integration of IF functions at the IC level, and dedicated multi-rate signal processors are now commercially available for use in next generation digital radios.

A chipset has been developed that can be used to design high sensitivity, low power digital radio receivers for a variety of Cellular and PCS standards, including AMPS, IS-136, PDC, GSM, and CDMA. The AD6600 is a dual channel, gain ranging receiver ADC that can provide 90 dB of dynamic range when sampling IF's signals as high as 250 MHz. It has on chip peak detectors, and RSSI. The AD6620 is a dual channel digital decimation programmable filter designed to interface directly with the AD6600 and subsequent DSPs. This chip can accept 16 bit input words at up to 65 MSPS; the decimated and filtered data can be accessed by serial or parallel words. The combination of high IF over-sampling with programmable digital filtering allows designers to replace many analog/RF functions with digital functions. The remainder of this paper will focus primarily on the high IF sampling receiver chip.

Section 2 describes the analog IF receiver chip.
Section 3 describes the digital filter chip.
Section 4 contains the system overview and conclusions.

2.0 Dual Channel ADC with RSSI and AGC

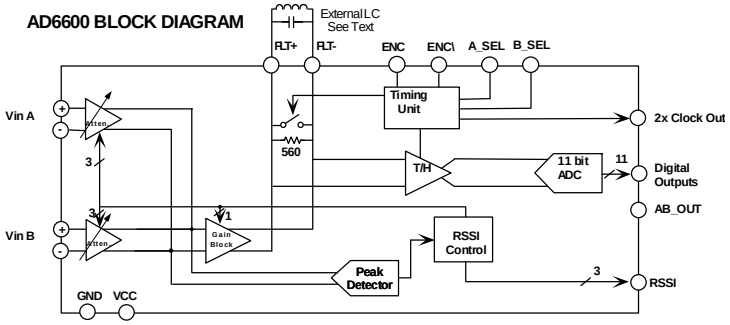

Figure 1: IF Sampling Receiver Block Diagram

Functional Description

The chip is designed to sample IF signals from 70 MHz to 250 MHz Ain at 20 MSPS. The two analog input pins, Vin A and Vin B, (see Figure 1) can be used to sample separate diversity antennas. A peak detector discerns the strength of each input signal and configures a series of on chip attenuators to match the received Ain to the full scale level of the ADC. The RSSI *(received signal strength indicator)* levels are communicated via a 3 bit digital word on a sample by sample basis synchronous with the ADC data. After the peak detectors, the signal paths are combined and brought off chip to a simple LC filter used to remove wide band noise. Coming back on chip, the signals are then digitized using a wide band and high dynamic range T/H and 11-bit ADC. The ADC is rated at 20 MSPS, and the user can control which input is digitized. Operating modes include A only, B only, or alternating A and B. At the rated IF frequencies, 90 dB of dynamic range is achieved: 30 dB from the gain ranging, and 60 dB from the 11-bit ADC. The AD6600 is

0-7803-4603-6/97/$5.00 (c) IEEE

built using a matched complementary bipolar process with NPN and PNP Ft's of 5.0 and 8.0 GHz respectively.

2.1 Peak Detector (RSSI) & Input attenuation (AGC)

The peak detector consists of a bank of high speed comparators and measures the magnitude of the input signal in the first 1/4 of the clock cycle (12.5 ns when operating the chip at 20MSPS.) To make an accurate measurement, the detector follows at least one half of an "IF" signals period. When operating at 20MSPS, the lowest IF that can accurately be sampled is 40 MHz; at 10 MSPS the lowest IF is 20 MHz. The limit for sampling high IFs is determined by the roll-off in the on-chip track and hold.

The peak detectors control the on board attenuators between 0 and -30 dB in 6 dB steps for each input channel. The matching between the gain settings is better than 0.5% and maintains a bandwidth of almost 1 GHz so the phase delay is small. Likewise the phase mismatches between different attenuator settings is very small, less than 0.2 degrees up to 200 MHz analog input. Additionally, the input impedance does not change with attenuator settings so there is no AM to PM distortion. The peak detector/attenuator circuitry acts as a real time RSSI/AGC loop that can greatly simplify system design.

2.2 Input Mode - A/B channel select

One ADC serves both attenuator inputs; the user can select which Ain signal is digitized by controlling an on-chip multiplexer. The sample rate of the ADC can be dedicated to either the A or B channel, or it can be used to alternately sample the A and B channels. In this final case, half of the ADC sample rate can be used to provide over-sampling, which limits the amount of processing gain that can be achieved in the subsequent decimation filter stages.

2.3 External Analog Filter

Since the analog front end has a bandwidth of nearly one gigahertz and the ADC a bandwidth of 500 MHz, a filter is required to bandwidth limit the wideband noise out of the attenuator and MUX stage. This simple external LC filter is tuned to the chosen IF frequency and is designed to settle quickly between clock cycles. To expedite settling between samples, an internal clamp circuit is utilized to discharge the filter. This minimizes feed through between inputs because of resonance in the filter stage. This is not an anti-aliasing filter which must be located prior to the AD6600.

2.4 ADC Operation

The ADC input is designed to take advantage of the excellent small signal linearity of the track and hold. Therefore the full scale input to the ADC section is 50 mV peak to peak. Other than this, the ADC section behaves much as any other ADC. The on-board track and hold is followed by an integrated gain block with a gain of four to increase the signal level to a level suitable for digitization with the 11 bit ADC. The track and hold has an input bandwidth of 450 MHz allowing accurate digitization of common IF frequencies up to 250 MHz. Once the signal is sampled with the track and hold, the frequency of the signal is reduced by the aliasing properties of the sampling process.

In order to minimize cross talk between the two IF inputs, a clamp circuit is employed that discharges the external LC filter and kills the gain of the drive amplifier between samples so that all samples start from mid-scale instead of the previous value which normally would be the IF signal of the previous sample. This effectively eliminates cross talk between samples.

2.5 IF sampling, aperture jitter, and over-sampling

The ADC has a sampling jitter of about 200 femto seconds, which is required to digitize high IF's with high dynamic range. With nearly full scale analog inputs, the observed SNR (with harmonics removed) is approximately 59 dB when digitizing 70 to 250 MHz Ain signals.

Many communications systems today have channel bandwidths ranging from 25 kHz (PDC) to 200 kHz (GSM). The high sample rate of the system allows significant over-sampling of the input signal, providing opportunities for processing gain in the subsequent digital stages. Another benefit coming from the combination of over-sampling and IF sampling is that harmonics and spurs can be positioned out of the analysis bandwidth thereby easing the requirements placed on RF mixers and IF amplifiers.

2.6 Digital Outputs

The digital outputs include a 3 bit digital RSSI word, the 11 bit ADC word. The 11-bit ADC output forms the mantissa of a binary floating point word, while the RSSI is the exponent. Figure 2 shows that the SNR stays in the 50 dB range for a wide variety of Ain levels. Below -32 dBm (-36dBfs), the minimum attenuation is activated and the SNR diminishes directly with the Ain level. Figures 3 & 4 demonstrate the operation of the chip for different attenuation levels at 155 MHz Ain.

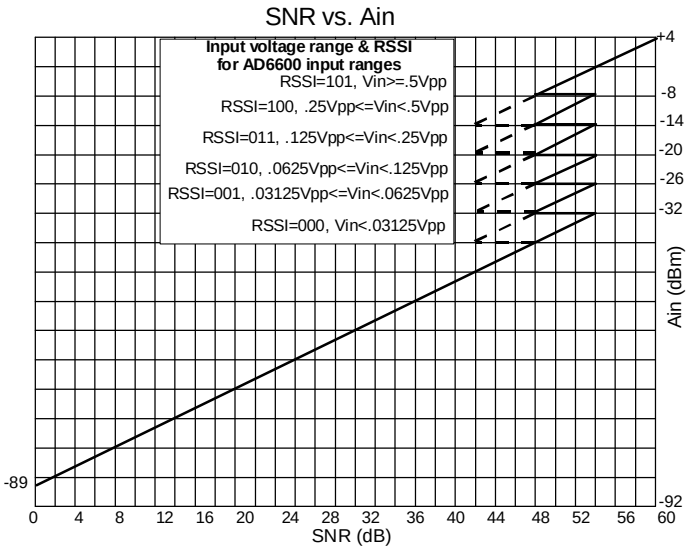

Figure 2: Ain level vs. SNR

The final digital output is an A/B channel indicator and a 2X clock output. The 2X clock output can be used to drive the subsequent digital filter; by doubling the clock rate of this chip, steeper filters can be generated, increasing receiver sensitivity.

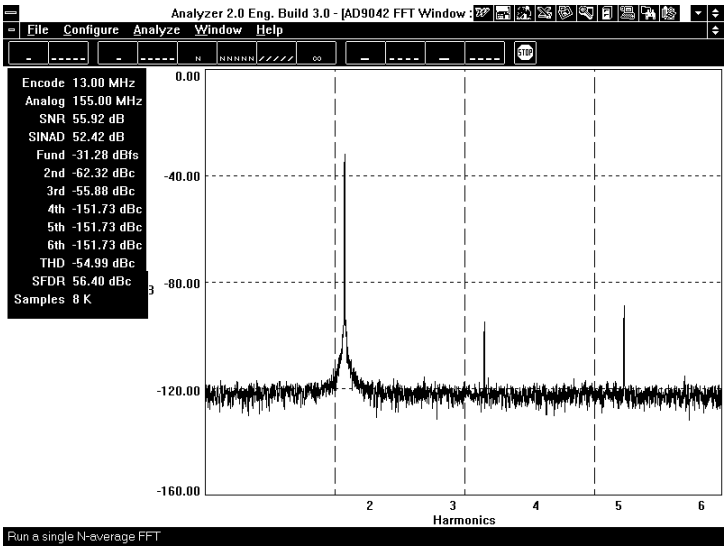

Figure 3. 13MSPS, 155 MHz Ain, Full Scale

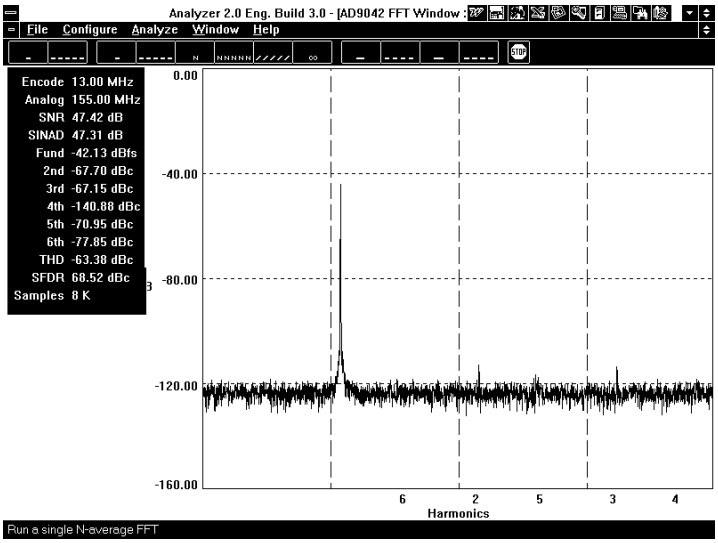

Figure 4: 13 MSPS, 155 MHz Ain, 5th gain range

3.0 Digital Filtering, Tuning, and Decimation

A digital filter chip was designed to accept the ADC + RSSI inputs data from the IF sampling chip. The first function accomplished is the conversion of the complex input word to a standard 16 bit word to facilitate the subsequent digital processing. The digital receiver chip consists of digital mixers with an NCO and three filter stages. See figure 5.

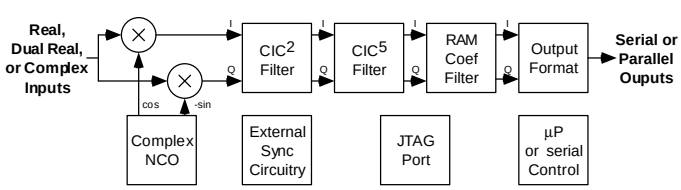

Figure 5: Digital Receiver Block Diagram

The digital mixer and numerically controlled oscillator (NCO) has a minimum dynamic range of 100 dB. The first filter and decimator is the CIC2 stage. This is a second order cascaded integrator comb (CIC) filter with fixed coefficients. The second filter stage is a fifth order cascaded integrator comb filter which also has fixed filter coefficients. The final filter stage is the RAM coefficient filter (|RCF). This stage is a programmable FIR filter and can be up to 256 taps long. All three filter stages can be used to distribute the decimation. Composite filter performance is a result of the three cascaded filter stages. For example, stop bands of better than 100 dB with transition bandwidths as low as 1 kHz can be achieved. The device can perform up to 1657 million math operations per second (Mops). This chip is designed to interface seamlessly with the IF sampling IC, as well as with most programmable DSPs. See Figure 6.

3.1 System Considerations for Digital Receivers

Digital receivers for a variety of Cellular and PCS standards can be easily developed using these recent technology advances. The overall sampling rate, IF filter characteristics, IF frequency selection, IF/RF gain distribution, and digital filter performance is determined by many factors, including the Tx/Rx frequencies, channel bandwidths, and system requirements. Figure 7 is a block diagram of a GSM receiver built using the IF sampling chip, providing receiver sensitivity in excess of 110 dB.

3.2 Benefits from Processing Gain

The high sample rate (20MSPS) of the ADC compared to the RF channel bandwidth allows significant over-sampling and subsequently large processing gain. Processing gain is defined as:

10 log (Sample rate/2*Channel BW).

Table 1 illustrates the amount of processing gain that can be obtained for several typical cellular and PCS examples. In the simplest case, the processing gain figure (in dB) can be added to the RSSI + ADC dynamic range provided by the IF sampling chip.

4.0 System Overview and Conclusion

Two new chips are described; the gain ranging and IF sampling ADC and a digital tuner and decimation filtering receiver chip. The AD6600 is built on a complementary bipolar process and provides 90 dB of instantaneous dynamic range when digitizing IF frequencies from 70 to 250 MHz. The AD6620 is a companion programmable digital filter that constructed in a standard 0.5 micron CMOS process and provides close in filtering and signal decimation. These chips can be used to construct single channel receivers for a variety of Cellular and PCS standards including CDMA, narrow band TDMA, and GSM.

Acknowledgements
The authors would like to thank the product development teams for both of these chips, including Carl Moreland, JJ Ray, Joe Young, Benny Chang, Michael Elliot, Steve Whitehead, Greg Harris, Benny McGlamery, Kevin Brown, Gloria McGlamery, Carroll Speir, Scott Behrhorst, Jeff Roehr, and Jeff Bray.

We would also like to sincerely thank our lead customers whose wisdom, patience and guidance have taught us much.

References:

Communications System Design, A/D Conversion, Dithering for Performance, Brad Brannon, Jan. 1997

EDN, Wide-dynamic-range A/D Converters Pave The Way For Wideband Digital-Radio Receivers, Brad Brannon November 1996

AD6600 Data Sheet - from Analog Devices
AD6620 Data Sheet - from Analog Devices

AN-501 Aperture Uncertainty and ADC System Performance, available from Analog Devices.

AN-502 GSM RF Front End Review with the AD6600, available from Analog Devices.

R.E. Crochiere, L.R. Rabiner: "Interpolation and decimation of Digital signals -- A tutorial review", Proc. IEEE, Vol. 69, No 3, March 1981

E.B. Hogenauer, "An economical class of digital filters for decimation and interpolation", IEEE Trans. Acoust. Speech, Signal Proc., vol. ASSP-29, pp.155-162 Apr. 1981

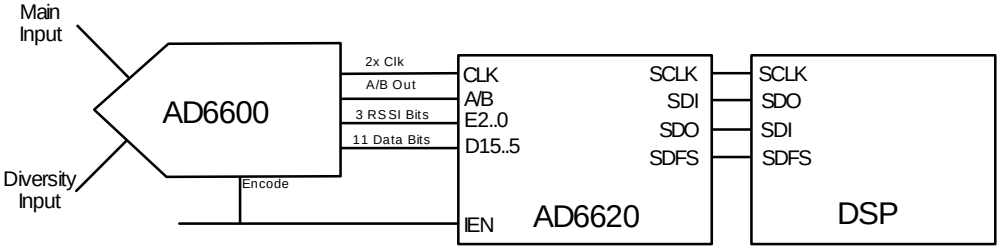

Figure 6: IF to filtered bits provided by AD6600 + AD6620 + DSP

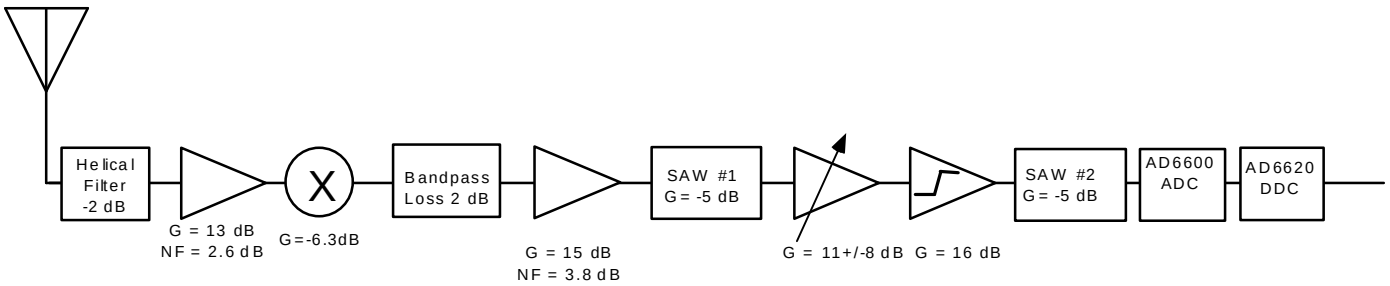

Figure 7: GSM Receiver - Illustrative Signal Chain

Standard	Channel BW	Data Rate	Sample rate	Processing Gain*
GSM	200 KHz	270.833 Kbit/sec	6.5 MSPS	12 dB
IS-136	30 KHz	48.6 Kbit/sec	9.72 MSPS	22 dB
PDC	25 KHz	42 Kbit/sec	8.40 MSPS	22 dB
CDMA	1.23 MHz	1.2288 Mbits/sec	19.66 MSPS	9 dB
PHS	300 KHz	384 Kbit/sec.	6.144 MSPS	10 dB

** Assumes 1 sample/symbol; some systems require multiple samples/symbol reducing processing gain.*

Table 1: Typical Processing Gain Obtained with AD6600 + AD6620